AMENDMENTS TO THE ABSTRACT

Please substitute the following paragraph(s) for the abstract now appearing in the currently filed specification:

-- ~~The present invention relates to the reducing of timing uncertainties in high-performance digital circuitry. More specifically, the present invention relates to a~~ A timing control ~~means~~ device and method for minimizing timing uncertainties due to skew and jitter, wherein a~~. A~~ ~~means~~ device for the compensation of timing errors in multiple channel electronic devices ~~comprising~~ comprises at least one register having a plurality of channels comprising: ~~comprises:~~ a clock for providing a clock signal; a reference signal generator for generating reference signals for deskewing the registers.~~; wherein for~~ For each ~~said~~ register, a corresponding feedback loop is associated for the relative alignment of the register's timing.~~, the~~ The feedback loop ~~comprising~~ comprises a ~~means~~ device for detecting a deviation from a predetermined level of probability of reading by ~~said~~ the register of a desired symbol on a boundary of two reference channel symbols in a sequence, and a set of delay devices ~~means~~ which use ~~uses~~ the detected values of probability to generate a feedback signal.

~~The invention is preferably implemented in a self-calibrated receiver and a self calibrating transmitter. Also, the invention can be employed in a digital interface between two items or within a circuit where there is a requirement for tight timing control such as requirement for a low skew between the channels of a register.~~ --